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*Linear integrated circuits gate questions solution EE141 -*

~~1/20/2012 Cross Section of CMOS Integrated Circuit | Lecture 21 |~~

~~EDC CMOS Inverter Cmos Digital Integrated Circuits Solutions~~

SOLUTION: (a) The AND and OR gates can be translated into CMOS circuit in the following steps: Solution Manual for CMOS

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CHAPTER 1 INTRODUCTION 1.1 47 2. 1.2 1.1 3. 1.3 4. 1.41.51.6

5. 1.7 6. Chapter 14 DESIGN FOR

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SOLUTION: (a) First find  $V_{OL}$ : the transistor operates in linear region when  $V_{out} = V_{OL}$ , therefore, The reasonable solution is :  
When  $V_{out} = V_{OH}$ , consider  $V_{IN} = 0$ , there is no current through load resistance. When  $V_{out} = V_{50\%}$ , (b) Transistor is off this case, see figure below.

*Solved > 6.2 Consider switching delays for 10 fF in a from ...*  
CMOS DIGITAL INTEGRATED CIRCUITS ANALYSIS AND DESIGN, Third Edition, By S. M. Kang and Y. Leblebici, McGraw Hill, 2002 or Forth Edition, 2015. Please click the above text title to check out the website developed to support the text. ON-LINE CADENCE TUTORIAL. Reference texts

*ESE570 Digital VLSI Circuits - Penn Engineering*  
CMOS Digital Integrated Circuits Analysis & Design Sung-Mo Kang Limited preview - 2014. CMOS Digital Integrated Circuits: Analysis and Design Sung-Mo Kang, Yusuf Leblebici Snippet view - 2003. CMOS Digital Integrated Circuits Analysis & Design Sung-Mo (Steve) Kang, Yusuf Leblebici Snippet view - 2002.

*Cmos Digital Integrated Circuits - Sung-Mo Kang, Yusuf ...*  
"CMOS Digital Integrated Circuits" 3rd Edition. by Sung-Mo Kang and Yusuf Leblebici; McGraw Hill, 2003. Time & Location. Cobleigh Hall 632 Tuesday, Thursday 11:00am - 12:15pm Pre-Requisites. EE262 - Logic Circuits Lab ; EE317 - Electronics; Weekly Schedule

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